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| EXAMINER | |
|---|---|
| CHANG, EDITH M | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/604,930 | ONO, SHIGERU | |
| | Examiner | Art Unit | |
| | Edith M Chang | 2634 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 1, 8, 15, 18, and 21 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4, 8-9, & 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiue et al. (US 6590872 B1) in view of Komatsu (US 5818882) and Kaku et al. (US 5550811).

Regarding **claims 1 & 8**, Except specifying (1) the CDMA receiver and detailing out (2) the frequency offset estimating section, Shiue et al. discloses: a receiver and its methods for a code division multiple access system comprising: *a pilot symbol producing section* (510-512-522-523-300 FIG.5) which produces pilot symbols of complex vector expression (FIG.3 wherein the I path presents the real part of the complex expression, the Q path presents the imaginary of the complex expression) from a received radio frequency (RF) signal based on a first local frequency signal (533 FIG.5, wherein the RF signal is converted to IF signal) and a second local frequency signal (531 FIG.5 wherein the signal is the I/Q baseband signal fed to the correlator to despread), *a frequency offset estimating section* (524 FIG.5); and *a local signal generating*

*section* which generates said first and second frequency signals based on said determined frequency offset (531-533 FIG.5).

With respect to item (1) the CDMA receiver, Komatsu teaches the CDMA receiver (column 1 lines 5-12). As Shiue et al. suggests the CDMA (column 1 lines 45-55), at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Shiue et al.'s receiver equipped with all basic elements to receive CDMA signal as a CDMA receiver with frequency offset correction ability taught by Komatsu reduced the quantity of computations and decrease the processing time for the computation to correct the frequency offset of CDMA signal (Abstract '882).

With respect item (2) the frequency offset estimating section, Komatsu teaches a frequency offset estimating section with the integration section (7-8 FIG.3 & FIG.5) and Kaku et al. teaches the details of the integration section (33-34 FIG.1, column 3 line 53-column 4 line 3). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the frequency offset detection taught by Komatsu implemented in Shiue et al.'s error estimators and the integrator taught by Kaku et al. to carry out in-phase adding operations to the pilot symbols of the complex vector expression over a predetermined interval in accordance with a predetermined pattern (33i-34i, 33q-34q FIG.1 '811), to carry out a complex adding operation of results of the in-phase adding operations (39 FIG.1 '811), and determines a frequency offset from a result of the complex adding operation (29 FIG.5 '882) .

The suggestion/motivation for doing so would have been optimized or improved signal reception and recovery/acquisition (column 4 lines 26-30 '872), reduced the quantity of computations and decrease the processing time for the computation to correct the frequency

offset (Abstract '882), and provided a precision sync acquisition and tracking circuit for a multi path DS/CDMA receiver (column 1 line 65-column 2 line47 '811).

Therefore, it would have been obvious to combine Kaku et al.'s integrators (33-34 FIG.1, column 3 line 53-column 4 line 3) with Komatsu's integration section (26 FIG.5), Komatsu's frequency offset detection and cancellation circuits (FIG.5 '882) with Shiue et al.'s error estimators (524 FIG.5 '872) to obtain the invention as specified in claims 1 and 8.

Regarding **claims 2 & 9**, Shiue et al. does not specify predetermined interval, Kaku et al. teaches the predetermined interval is an interval longer than one symbol period (column 3 lines 53-62, where the complex expression pilot symbols are summed over the period of m symbols where the m is the positive integer equal or greater than one). The combination as the rejection of claim 1 obtains the invention cited in claim 2.

Regarding **claims 4 & 11**, Shiue et al. does not specify the in-phase adding section, Kaku et al. teaches *an in-phase adding* section and its methods (33-34 of each demodulators FIG.1 '811) which carry out the in-phase adding operations to the pilot symbols of the complex vector expression over the predetermined interval in accordance with the predetermined pattern (column 3 line 53-column 4 line 3 wherein the predetermined pattern is from the 33 integrator, and the adding operations performed in 34 moving average circuit '811); *an addition synthesizing* section and its methods which carry out the complex adding operation (39 FIG.1 '811) of the results of the in-phase adding operations; and *a frequency offset estimating* unit and its methods (27-28-29-30 FIG.5 '882, refer the rejection of claim 1) which determine the frequency offset from the result of the complex adding operation.

4. Claims 3, 5-7, 10, 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiue et al. (US 6590872 B1) in view of Komatsu (US 5818882) and Kaku et al. (US 5550811) as applied claims 1 and 8 above, and further in view of Huang et al. (US 6266361).

Regarding **claims 3 & 10**, except explicitly specify to producing a channel count data indicative of a number of effective channels, Shiue et al. discloses all subject matter claimed: *the pilot symbol producing section* and its methods (510-512-522-523-300 FIG.5); and *the frequency offset estimating section* and its methods (524 FIG.5 wherein the summing pattern is the 33i-34i, 33q-34q FIG.1 '811 refer the rejection of claim 1). However Huang et al. teaches a channel count data indicative of *a number of effective channels* (column 7 lines 37-50, wherein the p paths from the matched filter greater than the threshold is the channel count data indicative of a number of effective channels). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the channel count data indicative of a number of effective channels taught by Huang et al. in Shiue et al.'s frequency offset estimating section to correct the frequency offset of a multipath fading presented in wideband CDMA channels (column 7 lines 36-37 '361).

Regarding **claims 5 & 12**, inheres the limitations of claims 4 and 8 respectively, Kaku et al. teaches in-phase adding section includes a plurality of *in-phase adding units* (33-34 FIG.1), each of which includes: *a buffer memory* which stores the pilot symbols of the complex vector expression (column 3 line 53-column 4 line 3, where the m-stage shift register of the adding unit is the memory); and *an in-phase adder* which reads out said pilot symbols of said complex vector expression from the buffer based on over the predetermined interval and the predetermined pattern, and carries out the in-phase adding operation to the read out pilot symbols

of the complex vector expression, and further Komatsu teaches a *control section* (20-21-23-24 FIG.5) which generates the predetermined interval and the predetermined pattern based on an addition count data indicative of a number of pilot symbols to be added and an in-phase summing pattern. The combination, refer to the rejection of claim 1, obtains the invention cited in the claims.

Regarding **claims 6 & 13**, Kaku et al. discloses a complex adder which carries out the complex adding operation of the results of the in-phase in the addition synthesizing section (39 FIG.1).

Regarding **claims 7 & 14**, inhering the limitations of claim 4 and claim 11 respectively, in the modified receiver of claims 4 and 11, further Katu discloses the frequency offset estimating unit includes: *a buffer memory* (33-34 FIG.1 '811) which stores the result of said complex adding operation; *a conjugate complex multiplier* (38 FIG.1 '811) which carries out a conjugate complex multiplication of the result of the complex adding operation stored in the buffer memory; further Komatsu discloses *an averaging unit* (26 FIG.5 '882, 33-34 FIG.1 '811) which carries out an averaging operation to the phase difference vectors; *an angle converter* (27 FIG.5, column 6 lines 45-55 '882) which converts the averaged phase difference vector to an angle value; *and a converter* (29 FIG.5, column 6lines 45-55 '882) which converts the angle value to the frequency offset based on a symbol rate.

5. Claims 15-18, & 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Komatsu (US 5818882) in view of Sato (US 5982763).

Regarding **claim 15**, except explicitly specify a frame format in which pilot symbols and data symbols are time multiplexed, Komatsu discloses: an automatic frequency controlling method in a code division multiple access system using a spectrum spreading technique comprising: *in-phase summing* (26 FIG.5) in the pilot symbols having a complex vector expression over a predetermined length of a symbol interval after converting the pilot symbols into the complex vector expression; and *estimating a frequency offset* (27-28-29 FIG.5) based on a result of conjugate complex multiplication of a plurality of said complex vector expressions which are subjected to the in-phase addition. However Sato teaches a frame format in which pilot symbols and data symbols are time multiplexed for transmission and in which a variable transmission symbol rate is realized by making a spreading rate variable under a constant chip rate (FIG.2) and having at least two different in-phase summation rates the pilot symbols (FIG.8, where the PL(i) i=0 to Np-1, the PL period can have at least two PL symbols when Np-1= 1) that the in-phase sums in at least two different in-phase summation rate the pilot symbols. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the frame format with different pilot symbols in the pilot frame so that to have different in-phase summation rates the pilot symbols, taught by Sato in Komatsu's frequency offset cancellation apparatus to receive CDAM signals which comprises pilot symbols and data symbols to reduce the frequency offset, thus to improve reception quality of the receiver (column 3 lines 10-15 '763).

Regarding **claim 16**, Komatsu discloses the *controlling* an oscillation frequency of a crystal oscillator in accordance with an estimation of the frequency offset calculated through the estimation of the frequency offset (90-91 FIG.1); *converting* the received frequency signal into an intermediate frequency signal in accordance with the oscillation frequency (BB FIG.1, where the RF converted to IF, then to baseband); and orthogonally *demodulating* the intermediate frequency signal based on the oscillation frequency (93-94-95 FIG.1).

**Regarding claim 17**, except explicitly specify an in-phase component and an orthogonal component, Komatsu discloses: the *obtaining a baseband* signal (Abstract) having an in-phase component and an orthogonal component through the orthogonal modulation and converting into digital signals by A/D converters (1-3 FIG.3), respectively; *inversely spreading* the digital signals (4-7-8 FIG.3) by inversely spreading units to separate the pilot symbols from the data symbols (20-24 FIG.5 to separate the pilot signal); and *converting* the pilot symbols into complex vector expressions by canceling the data modulated components of the pilot signals (7-8 FIG.5). However Sato teaches the in-phase component and the orthogonal component (column 4 lines 58-61). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the in-phase component and the orthogonal component taught by Sato to have the complex number representative of the symbol to require least computation amount.

Regarding **claim 18**, except explicitly specify a frame format in which pilot symbols and data symbols are time multiplexed and an in-phase component and an orthogonal component in a baseband signal, Komatsu discloses all subject matters claimed: an automatic frequency controlling system in a code division multiple access system using a spectrum spreading technique comprising: *an orthogonal demodulator* converting a received signal into a baseband

signal (90, BB FIG.1); *inversely spreading units* inversely spreading the in-phase component and the orthogonal component of the baseband signal; *pilot symbol interval detectors* (20-24 FIG.5) separating the pilot symbols from the data symbols; inverse demodulating units (A-N Fig.3) converting the pilot symbols into complex vector expressions by canceling data modulated components of the pilot symbols; *an in-phase summing section* (26 FIG.5) in-phase summing in at least two different manners; and *an estimating section* (27-29 FUG,5) estimating the frequency offset from conjugate complex multiplication of a plurality of said complex vector expressions which are subjected to the in-phase summation. However Sato teaches a frame format in which pilot symbols and data symbols are time multiplexed for transmission and in which a variable transmission symbol rate is realized by making a spreading rate variable under a constant chip rate (FIG.2) and having at least two different in-phase summation rates the pilot symbols (FIG.8, where the PL(i) i=0 to Np-1, the PL period can have at least two PL symbols when Np-1= 1, the pilot frame can have more than one symbols that provides different in-phase summation rates the pilot symbols); and the in-phase component and the orthogonal component (column 4 lines 58-61). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the frame format and the in-phase component and the orthogonal component taught by Sato in Komatsu's frequency offset cancellation apparatus to receive CDAM signals which comprises pilot symbols and data symbols to reduce the frequency offset and its computation amount, thus to improve reception quality of the receiver (column 3 lines 10-15 '763).

Regarding **claim 20**, Komatsu discloses *a controlling section* controlling the oscillation frequency of a crystal oscillator in accordance with an estimation of the frequency offset obtained through the estimation of the frequency offset (91-92 FIG.1); and a *converting*

*section* (90 FIG.1 where the RF signal converted to IF, then the baseband orthogonal demodulated signal that is the inhering of the frequency conversion circuit/radio reception section/RF front-end of the CDAM wireless mobile system) converting the received frequency signal into an intermediate frequency signal in accordance with the oscillation frequency, wherein the intermediate frequency signal is orthogonally demodulated using the oscillation frequency.

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Komatsu (US 5818882) in view of Sato (US 5982763), further in view of Kaku et al. (US 5550811).

Regarding **claim 19**, Komatsu discloses *a buffer memory* storing the symbols over at least two symbol intervals of the complex vector signal received from the demodulator (23 FIG.5 where the n=2); and *an in-phase adder* in-phase summing the outputs of the buffer memory (26 FIG.5), and *the estimating section* estimating the frequency offset (26-30 FIG.5), comprising an *angle/frequency offset converter* averaging and converting outputs of the conjugate complex multiplier into angular components, and converting the angular components into frequency components to estimate a frequency offset (27-29 FIG.5), HOWEVER does not specify a complex adder, a conjugate complex multiplier.

Kaku et al. teaches *a complex adder* (33-34 FIG.1) and a *conjugate complex multiplier* (38 FIG.1) as cited in the claim. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the integrators/moving average circuits taught by Kaku et al. implemented in Komatsu's integrator to reduced the quantity of computations and decrease the processing time for the computation to correct the frequency offset (Abstract '822), and

provided a precision sync acquisition and tracking circuit for a multi path DS/CDMA receiver (column 1 line 65-column 2 line47 '811).

7. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiue et al. (US 6590872 B1) in view of Komatsu (US 5818882) and Kaku et al. (US 5550811), further in view of Sato (US 5982763).

Regarding **claim 21**, Shieu et al. discloses a receiver equipped to receive CDAM signal, comprising: *a mixer* for converting a received frequency signal into an intermediate frequency signal (510 FIG.5 where the RF circuitry converts the RF signal to IF signal); *a first local frequency generator* supplying the mixer with a local oscillation signal (533 FIG.5); *an orthogonal demodulator* (523-531 FIG.5) for orthogonally demodulating the intermediate frequency signal in accordance with a second local frequency of a second local frequency generator; *inversely spreading units* (300 FIG.5) converting in-phase components and orthogonal components of the baseband signal received from the orthogonal demodulator into analog/digital signals; and the error estimator, HOWEVER Shieu et al. does not explicitly specify the receiver is a CDMA receiver, the frame format; the pilot symbol demodulators, and the in-phase adders.

Komatsu teaches the CDMA receiver (column 1 lines 5-12). As Shiue et al. suggests the CDMA (column 1 lines 45-55), at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Shiue et al.'s receiver equipped with all basic elements to receive CDMA signal as a CDMA receiver with frequency offset correction ability taught by Komatsu reduced the quantity of computations and decrease the processing time for the computation to correct the frequency offset of CDMA signal (Abstract '882).

Sato teaches a frame format in which pilot symbols and data symbols are time multiplexed for transmission and in which a variable transmission symbol rate is realized by making a spreading rate variable under a constant chip rate (FIG.2) and having at least two different in-phase summation rates the pilot symbols (FIG.8, where the PL(i) i=0 to Np-1, the PL period can have at least two PL symbols when Np-1= 1); Komatsu teaches a frequency offset estimating section with the integration section (7-8 FIG.3 & FIG.5) and *pilot symbol demodulators* separating the inversely spread signal outputted from the inversely spreading units into pilot symbols and data symbols; and Kaku et al. teaches the details of the integration section (33-34 FIG.1, column 3 line 53-column 4 line 3). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have *the frequency offset estimator* taught by Komatsu implemented in Shiue et al.'s error estimators, the *in-phase adders/averaging circuits* taught by Kaku et al. in Komatsu's integration section, and to have the pilot and data multiplexed frame format taught by Sato in Komatsu's frequency offset cancellation apparatus, to carry out in-phase adding operations to the pilot symbols of the complex vector expression over a predetermined interval in accordance with a predetermined pattern (33i-34i, 33q-34q FIG.1 '811), to carry out a complex adding operation of results of the in-phase adding operations (39 FIG.1 '811), to determine a frequency offset from a result of the complex adding operation (29 FIG.5 '882), to receive CDAM signals which comprises pilot symbols and data symbols (column 3 lines 10-15 '763).

The suggestion/motivation for doing so would have been optimized or improved signal reception and recovery/acquisition (column 4 lines 26-30 '872), reduced the quantity of computations and decrease the processing time for the computation to correct the frequency

offset (Abstract '822), and provided a precision sync acquisition and tracking circuit for a multi path DS/CDMA receiver (column 1 line 65-column 2 line47 '811), reduced the frequency offset, thus improved reception quality of the receiver (column 3 lines 10-15 '763).

Therefore, it would have been obvious to combine Kaku et al.'s integrators (33-34 FIG.1, column 3 line 53-column 4 line 3) with Komatsu's integration section (26 FIG.5), Sato's pilot and data multiplexed frame teaching (FIG.2 & 8 '763) with Komatsu's frequency offset detection and cancellation circuits (FIG.5 '882); Komatsu's frequency offset detection and cancellation circuits (FIG.5 '882) with Shiue et al.'s error estimators (524 FIG.5 '872) to obtain the invention as specified in claim 21.

***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 703-305-3416. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
April 5, 2004

CHIEH M. FAN
PRIMARY EXAMINER